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Carter, J.N.; Smart, R.G.; Tropper, A.C.; Hanna, D.C.; Carter, S.F.; Szebesta, D.;
Lightwave Technology, Journal of
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Carter, T.; Carter, A.;
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Smart, R.G.; Tropper, A.C.; Hanna, D.C.; Carter, J.N.; Davey, S.T.; Carter, S.F.; Szebesta, D.;
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Smart, R.G.; Carter, J.N.; Tropper, A.C.; Hanna, D.C.; Carter, S.F.; Szebesta, D.;
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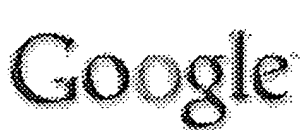
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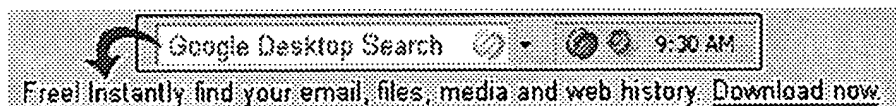
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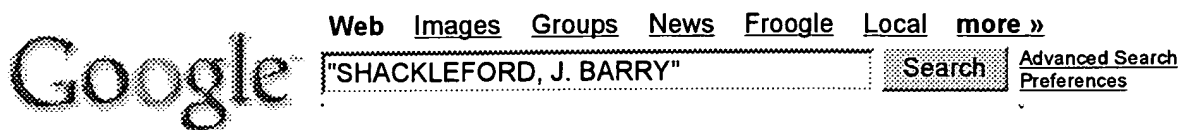
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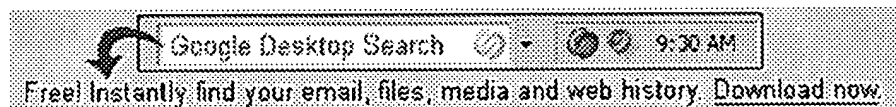
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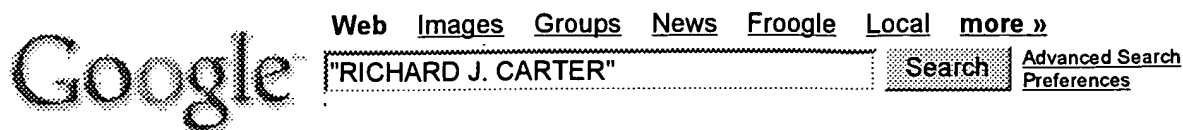
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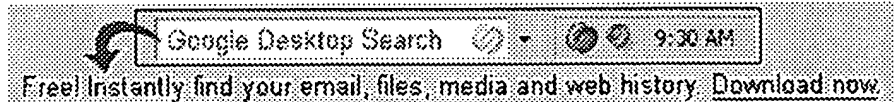
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Barry Shackelford, Motoo Tanaka, Richard J. Carter, Greg Snider

 February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**

Full text available: pdf(565.95 KB)

 Additional Information: [full citation](#), [abstract](#), [references](#)

Random number generators (RNGs) based upon neighborhood-of-four cellular automata (CA) with asymmetrical, non-local connections are explored. A number of RNGs that pass Marsaglia's rigorous Diehard suite of random number tests have been discovered. A neighborhood size of four allows a single CA cell to be implemented with a four-input lookup table and a one-bit register which are common building blocks in popular field programmable gate arrays (FPGAs). The investigated networks all had periodic ...

Keywords: FPGA, cellular automata, random number generator

2 [Attacking the semantic gap between application programming languages and configurable hardware](#)

Greg Snider, Barry Shackelford, Richard J. Carter

 February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**

Full text available: pdf(258.65 KB)

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It is difficult to exploit the massive, fine-grained parallelism of configurable hardware with a conventional application programming language such as C, Pascal or Java. The difficulty arises from the mismatch between the synchronous, concurrent processing capability of the hardware and the expressiveness of the language-the so-called "semantic gap." We attack this problem by using a programming model matched to the hardware's capabilities that can be implemented in any (unmodified) object ...

3 [Cube-4—a scalable architecture for real-time volume rendering](#)

Hanspeter Pfister, Arie Kaufman

 October 1996 **Proceedings of the 1996 symposium on Volume visualization**

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4 Plasma: an FPGA for million gate systems

R. Amerson, R. Carter, W. Culbertson, P. Kuekes, G. Snider, Lyle Albertson

February 1996 **Proceedings of the 1996 ACM fourth international symposium on Field-programmable gate arrays**

Full text available:  [pdf\(264.25 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

Keywords: FPGA, custom computing, register files

5 Spatial computation

Mihai Badiu, Girish Venkataramani, Tiberiu Chelcea, Seth Copen Goldstein

October 2004 **Proceedings of the 11th international conference on Architectural support for programming languages and operating systems**, Volume 32 , 39 , 38 Issue 5 , 11 , 5

Full text available:  [pdf\(573.00 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper describes a computer architecture, *Spatial Computation* (SC), which is based on the translation of high-level language programs directly into hardware structures. SC program implementations are completely distributed, with no centralized control. SC circuits are optimized for *wires* at the expense of computation units. In this paper we investigate a particular implementation of SC: ASH (Application-Specific Hardware). Under the assumption that computation is cheaper than co ...

Keywords: application-specific hardware, dataflow machine, low-power, spatial computation

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